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EXAMINER	
GRAYBILL, DAVID E	
ART UNIT	**PAPER NUMBER**
2822	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/852,824	LIN, CHARLES W.C.	
	Examiner	Art Unit	
	David E Graybill	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15-119* is/are pending in the application.

4a) Of the above claim(s) *17,21,31-34,39,41-44,50-54,62-65,80-84 and 105-109* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15,16,18-20,22-30,35-38,40,45-49,55-61,66-79,85-104 and 110-119* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10 pages*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 20, 24, 25-30, 35-38, 40, 45-49, 55, 56-61, 66-71, 73-79, 85-94, 96-104 and 110-119 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The undescribed subject matter is the following negative limitations:

Claim 20, "without filling a top portion of the via hole after the reflowing";

Claim 24, "are the only materials in the via hole after the reflowing";

Claims 25 and 55, "prevents the via hole from exposing the pad";

Claim 46, "without filling a top portion of the via hole";

Claim 59, "are the only materials in the via hole after applying the heat";

Claim 60, "does not contact the solder on the bond site," "does not contact the pad," "does not contact the chip," and, "does not contact the solder joint and does not contact the chip";

Claim 68, "are the only materials in the via hole after applying the heat to reflow the solder";

Claims 70, 71, 75, 76, 85, 86, 90 and 91, "does not electrically connect the substrate and the chip";

Claims 73, 78, 88 and 93, "a solder-free pad";

Claims 74, 79, 89 and 94, "solder-free pad";

Claim 96, "is the only material in the via hole that contacts the metallization after the reflowing";

Claim 97, "is the only material in the via hole that contacts the pad after the reflowing";

Claim 98, "is the only material that contacts the metallization and the pad after the reflowing";

Claim 99, "is the only conductor external to the chip that contacts the pad after the reflowing";

Claim 101, "is the only material in the via hole that contacts the metallization";

Claim 102, "is the only material in the via hole that contacts the pad";

Claim 103, "is the only material that contacts the metallization and the pad";

Claim 104, "is the only conductor external to the chip that contacts the pad";

Claim 111, "is the only material in the via hole that contacts the metallization";

Claim 112, "is the only material in the via hole that contacts the pad";

Claim 113, "is the only material that contacts the metallization and the pad";

Claim 114, "is the only conductor external to the chip that contacts the pad";

Claim 116, "is the only material in the via hole that contacts the metallization";

Claim 117, "is the only material in the via hole that contacts the pad";

Claim 118, "is the only material that contacts the metallization and the pad";

Claim 119, "is the only conductor external to the chip that contacts the pad."

To further clarify, any negative limitation or exclusionary proviso must have basis in the original disclosure. See Ex parte Grasselli, 231 USPQ 393 (Bd. App. 1983) aff'd mem., 738 F.2d 453 (Fed. Cir. 1984). The mere absence of a positive recitation is not basis for an exclusion.

Claims 15, 16, 18-20, 22-30, 35-38, 40, 45-49, 55, 56, 59-61, 66, 68, 70-79, 85-104 and 110-119 are rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling.

Specifically, claims 57, 58, 67 and 69, recite essential limitations preceded by the term "essentially," however, claims 15, 16, 18-20, 22-30, 35-38, 40, 45-49, 55, 56, 59-61, 66, 68, 70-79, 85-104 and 110-119 fail to recite these essential limitations. A claim that omits an element which applicant describes as an essential or critical feature of the invention originally disclosed does not comply with the written description requirement. See Gentry Gallery, 134 F.3d at 1480, 45 USPQ2d at 1503; In re Sus, 306 F.2d 494, 504, 134 USPQ 301, 309 (CCPA 1962). A claim which omits matter disclosed to be essential to the invention as described in the specification or in other statements of record may also be subject to rejection under 35 U.S.C. 112, para. 1, as not enabling, or under 35 U.S.C. 112, para. 2. See In re Mayhew, 527 F.2d 1229, 188 USPQ 356 (CCPA

1976); In re Venezia, 530 F.2d 956, 189 USPQ 149 (CCPA 1976); and In re Collier, 397 F.2d 1003, 158 USPQ 266 (CCPA 1968). See also MPEP § 2163IB and § 2172.01.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 57, 58, 67 and 69 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The scopes of the claims are unclear because the term "essentially" appears to be given a meaning repugnant to its usual meaning. To further clarify, this rejection is made in view of applicant's remarks filed on 10-1-4, wherein, at page 18, lines 5 and 12, applicant appears to improperly define the term *essentially* as "a vast majority."

In the rejections infra, generally, reference labels are recited only for the first recitation of identical claim elements.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 15, 16, 18-20, 22-30, 36-38, 45-49, 70-79 and 95-104 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Hino (6157084).

At column 4, line 19 to column 5, line 56; column 7, lines 10-16; column 7, line 65 to column 8, line 31; and column 9, lines 1-30, Hino discloses the following:

A method of making a flip chip assembly, comprising: attaching a substrate 2 to a semiconductor chip 3, wherein the substrate includes a dielectric layer 6 and metallization 5, 7, 8 and 13, the dielectric layer includes first 6b and second 6a surfaces that are opposite one another and a

via hole (the hole filled by 5, 7, 8 and 13) that extends between the first and second surfaces, the metallization is disposed on walls of the via hole and extends along the walls to the first and second surfaces, the chip includes a terminal pad 12 that is aligned with the via hole, and a reflowable material 15 that contains solder contacts the metallization and the pad; and then reflowing the reflowable material to provide an electrical connection between the metallization and the pad; wherein the reflowable material is deposited on the metallization before attaching the substrate to the chip, and during the reflowing the reflowable material wets and flows on an exposed portion of the pad beneath the via hole; wherein the pad is directly beneath substantially all surface area defined by the via hole after the attaching; wherein the metallization is electrolessly plated on the walls of the via hole; wherein the reflowable material fills a bottom portion of the via hole without filling a top portion of the via hole after the reflowing; wherein the substrate remains at a fixed position relative to the chip during the reflowing; wherein substantially all of the reflowable material is within the via hole after the reflowing "the conductive paths 7 and 8 are formed only to reach the same surface level with both surfaces 6a and 6b"; wherein the metallization and the reflowable material are the only materials in the via hole after the

reflowing; attaching the substrate to the chip using an adhesive that does not electrically connect the substrate and the chip; attaching the substrate to the chip using an adhesive that is sandwiched between and contacts the substrate and the chip and does not electrically connect the substrate and the chip; wherein the pad is a bumpless pad; wherein the pad is a solder-free pad; wherein the pad is a bumpless solder-free pad; wherein the reflowable material extends continuously between the first and second surfaces in the via hole after the reflowing; wherein the reflowable material is the only material in the via hole that contacts the metallization after the reflowing; wherein the reflowable material is the only material in the via hole that contacts the pad after the reflowing; wherein the reflowable material is the only material that contacts the metallization and the pad after the reflowing; wherein the reflowable material is the only conductor external to the chip that contacts the pad after the reflowing.

A method of making a flip chip assembly, comprising the following steps in the sequence set forth: providing a substrate that includes a dielectric layer, wherein the dielectric layer includes first and second surfaces that are opposite one another and a via hole that extends between the first and second surfaces; depositing metallization (at least 7, 8 and 13)

on walls of the via hole such that the metallization extends along the walls to the first and second surface; depositing solder on the metallization such that the solder is disposed in the via hole; attaching the substrate to a semiconductor chip that includes a terminal pad, wherein the first surface faces away from the chip, the second surface faces towards the chip, the via hole is aligned with the pad and the solder contacts the pad; and applying heat to reflow the solder to form a solder joint that contacts and electrically connects the metallization and the pad and prevents the via hole from exposing the pad; depositing the metallization on the walls using electroless plating; depositing the metallization on the walls such that substantially all of the metallization is within the via hole; depositing the metallization on the walls such that the metallization provides a plated through-hole; depositing the metallization on the walls such that the metallization is aligned with the second surface; depositing the solder on the metallization using electroplating; attaching the substrate to the chip such that the via hole exposes the pad (to 7); attaching the substrate to the chip such that the pad is directly beneath substantially all surface area defined by the via hole; attaching the substrate to the chip using an adhesive 20 between the substrate and the chip; applying the heat to reflow the solder such that

substantially all of the solder joint is within the via hole; applying the heat to reflow the solder such that the solder joint fills a bottom portion of the via hole without filling a top portion of the via hole; applying the heat to reflow the solder such that the solder wets and covers an exposed portion of the pad; applying the heat to reflow the solder while maintaining the substrate at a fixed position relative to the chip; wherein the metallization and the solder joint are the only materials in the via hole after applying the heat; attaching the substrate to the chip using an adhesive that does not electrically connect the substrate and the chip; attaching the substrate to the chip using an adhesive that is sandwiched between and contacts the substrate and the chip and does not electrically connect the substrate and the chip; wherein the pad is a bumpless pad; wherein the pad is a solder-free pad; wherein the pad is a bumpless solder-free pad; wherein the solder joint extends continuously between the first and second surfaces in the via hole; wherein the solder joint is the only material in the via hole that contacts the metallization; wherein the solder joint is the only material in the via hole that contacts the pad; wherein the solder joint is the only material that contacts the metallization and the pad; wherein the solder joint is the only conductor external to the chip that contacts the pad.

To further clarify the disclosure of the pad beneath the via hole, the pad is directly beneath the via, and the reflowable material fills a bottom portion of the via hole without filling a top portion, the disclosed process of Hino is not limited to an absolute frame of reference or otherwise limited to a particular orientation, and it is inherent that there is a frame of reference wherein the pad is beneath the via hole, the pad is directly beneath the via, and the reflowable material fills a bottom portion of the via hole without filling a top portion.

To further clarify the disclosure wherein the substrate remains at a fixed position relative to the chip during the reflowing, this process is an inherent property of the embodiment wherein "the conductive paths 7 and 8 are formed only to reach the same surface level with both surfaces 6a and 6b." Also, in the embodiment of FIG. 9, the substrate remains at a fixed position in the horizontal direction relative to the chip during the reflowing.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 40 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hino as applied to claim 25, and further in combination with Gaynes (6165885).

Hino does not appear to explicitly disclose applying the heat to reflow the solder using a convection oven.

Nonetheless, at column 21, lines 15-17, Gaynes discloses applying heat to reflow solder using a convection oven. Moreover, it would have been obvious to combine this process of Gaynes with the process of Hino because it would facilitate the reflow of Hino.

Claims 15, 16, 18, 20, 23, 24, 70-74 and 95-99 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vinciarelli (5526234) and Moden (5920123).

At column 8, lines 15-65, Vinciarelli discloses a method of making a flip chip assembly, comprising: attaching a substrate to another substrate, wherein the substrate inherently includes a dielectric layer 17 and metallization (the portion of 77 within the via hole), the dielectric layer includes first and second surfaces that are opposite one another and a via hole 45a that extends between the first and second surfaces, the metallization is disposed on walls of the via hole and extends along the walls

to the first and second surfaces, the another substrate includes a terminal pad 71 that is aligned with the via hole, and a reflowable material 79 that contains solder contacts the metallization and, at least indirectly, the pad; and then reflowing the reflowable material to provide an electrical connection between the metallization and the pad; wherein the reflowable material is at least indirectly deposited on the metallization before attaching the substrate to the chip, and during the reflowing the reflowable material wets and flows on an exposed portion of the pad beneath the via hole; wherein the pad is directly beneath substantially all surface area defined by the via hole after the attaching; wherein the reflowable material fills a bottom portion of the via hole without filling a top portion of the via hole after the reflowing; wherein substantially all of the reflowable material is within the via hole after the reflowing; wherein the metallization and the reflowable material are the only materials in the via hole after the reflowing; wherein the pad is a bumpless pad (at least before it is aligned with the via hole); wherein the pad is a solder-free pad (at least before it is aligned with the via hole); wherein the pad is a bumpless solder-free pad (at least before it is aligned with the via hole); wherein the reflowable material extends continuously between the first and second surfaces in the via hole after the

reflowing; wherein the reflowable material is the only material in the via hole that contacts the metallization after the reflowing; wherein the reflowable material is the only material in the via hole that contacts the pad after the reflowing; wherein the reflowable material is the only material that contacts the metallization and the pad after the reflowing; wherein the reflowable material is the only conductor external to the chip that contacts the pad after the reflowing.

To further clarify, the substrate inherently includes a dielectric layer 17 because Vinciarelli discloses that the substrate is a printed circuit board, and the Manual of Classification, Class 438, Glossary, defines a printed circuit board as, "A structure formed on one or more layers of electrically insulating material . . . ."

However, Vinciarelli does not appear to explicitly disclose that the another substrate is a semiconductor chip; attaching the substrate to the chip using an adhesive that does not electrically connect the substrate and the chip; attaching the substrate to the chip using an adhesive that is sandwiched between and contacts the substrate and the chip and does not electrically connect the substrate and the chip.

Nonetheless, at column 2, line 38 to column 4, line 22; and column 5, lines 37-40, Moden discloses a semiconductor chip "integrated circuit chip" 16, attaching the substrate 12 to the chip using an adhesive 27 that does not electrically connect the substrate and the chip; attaching the substrate to the chip using an adhesive that is sandwiched between and contacts the substrate and the chip and does not electrically connect the substrate and the chip. Moreover, it would have been obvious to combine this disclosure of Moden with the disclosure of Vinciarelli because it would facilitate electrical connection to a semiconductor chip.

Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Vinciarelli and Moden as applied to claim 15, and further in combination with Saito (JP63194342).

Vinciarelli and Moden do not appear to explicitly disclose wherein the substrate remains at a fixed position relative to the chip during the reflowing.

Nevertheless, in the English abstracts and Figures, Saito discloses wherein the substrate 1 remains at a fixed position relative to the chip 3 during the reflowing. Furthermore, it would have been obvious to combine

this disclosure of Saito with the disclosure of the applied prior art because it would facilitate the alignment and reflowing of the applied prior art.

Claims 19, 25-30, 35-38, 45-47, 49, 55-59, 75-79, 85-89, 100-104 and 110-114 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vinciarelli and Moden as applied to claims 15, 16, 18, 20, 23, 24, 70-74 and 95-99, and further in combination with Mazzoni (5863406).

As cited supra, Vinciarelli and Moden disclose the following: A method of making a flip chip assembly, comprising the following steps in the sequence set forth: providing a substrate that includes a dielectric layer, wherein the dielectric layer includes first and second surfaces that are opposite one another and a via hole that extends between the first and second surfaces; depositing metallization on walls of the via hole such that the metallization extends along the walls to the first and second surfaces; depositing solder at least indirectly on the metallization; attaching the substrate to a semiconductor chip that includes a terminal pad, wherein the first surface faces away from the chip, the second surface faces towards the chip, the via hole is aligned with the pad and the solder at least indirectly contacts the pad; and applying heat to reflow the solder to form a solder joint that contacts and electrically connects the metallization and the pad

and prevents the via hole from exposing the pad; depositing the metallization on the walls such that substantially all of the metallization is within the via hole; depositing the metallization on the walls such that the metallization provides a plated through-hole; depositing the metallization on the walls such that the metallization is aligned with the second surface; attaching the substrate to the chip such that the via hole exposes the pad; attaching the substrate to the chip such that the pad is directly beneath substantially all surface area defined by the via hole; attaching the substrate to the chip using an adhesive between the substrate and the chip; applying the heat to reflow the solder such that substantially all of the solder joint is within the via hole; applying the heat to reflow the solder such that the solder joint fills a bottom portion of the via hole without filling a top portion of the via hole; applying the heat to reflow the solder such that the solder wets and covers an exposed portion of the pad; wherein the metallization and the solder joint are the only materials in the via hole after applying the heat; attaching the substrate to the chip using an adhesive that does not electrically connect the substrate and the chip; attaching the substrate to the chip using an adhesive that is sandwiched between and contacts the substrate and the chip and does not electrically connect the substrate and

the chip; wherein the pad is a bumpless pad; wherein the pad is a solder-free pad; wherein the pad is a bumpless solder-free pad; wherein the solder joint extends continuously between the first and second surfaces in the via hole; wherein the solder joint is the only material in the via hole that contacts the metallization; wherein the solder joint is the only material in the via hole that contacts the pad; wherein the solder joint is the only material that contacts the metallization and the pad; wherein the solder joint is the only conductor external to the chip that contacts the pad.

A method of making a flip chip assembly, comprising the following steps in the sequence set forth: providing a substrate that includes a dielectric layer, wherein the dielectric layer includes first and second surfaces that are opposite one another and a via hole that extends between the first and second surfaces; electrolessly plating metallization on walls of the via hole, wherein the metallization extends along the walls to the first and second surfaces; forming solder at least indirectly on the metallization; attaching the substrate to a semiconductor chip using an adhesive therebetween, wherein the first surface faces away from the chip, the second surface faces towards the chip, the chip includes a terminal pad, the via hole is aligned with and exposes the pad, the solder at least indirectly

contacts the pad and the metallization is spaced from the pad; and applying heat to reflow the solder such that the solder wets and flows on the pad and forms a solder joint that contacts and electrically connects the metallization and the pad and prevents the via hole from exposing the pad; wherein the metallization is aligned with the second surface; wherein essentially all of the solder joint is in the via hole; wherein the pad is directly beneath essentially all surface area defined by the via hole after attaching the substrate to the chip; wherein the metallization and the solder joint are the only materials in the via hole after applying the heat; attaching the substrate to the chip using an adhesive that does not electrically connect the substrate and the chip; attaching the substrate to the chip using an adhesive that is sandwiched between and contacts the substrate and the chip and does not electrically connect the substrate and the chip; wherein the pad is a bumpless pad; wherein the pad is a solder-free pad; wherein the pad is a bumpless solder-free pad; wherein the solder joint extends continuously between the first and second surfaces in the via hole; wherein the solder joint is the only material in the via hole that contacts the metallization; wherein the solder joint is the only material in the via hole that contacts the pad; wherein the solder joint is the only material that contacts the

metallization and the pad; wherein the solder joint is the only conductor external to the chip that contacts the pad.

However, Vinciarelli and Moden do not appear to explicitly disclose depositing solder on the metallization such that the solder is disposed in the via hole; depositing the metallization on the walls using electroless plating; depositing the solder on the metallization using electroplating; depositing the solder on the metallization such that solder extends along the metallization to the first and second surfaces.

Regardless, at column 1, lines 6-41 and 53-55; column 2, lines 1-7; column 4, line 3 to column 6, line 37; and column 6, lines 51-59; Mazzoni discloses, depositing solder 340 on the metallization such that the solder is disposed in the via hole 140; depositing the metallization 310 on the walls using electroless plating; depositing the solder on the metallization using electroplating; depositing the solder on the metallization such that solder extends along the metallization to the first and second surfaces. In addition, it would have been obvious to combine this disclosure of Mazzoni with the disclosure of the applied prior art because it would facilitate application of the solder to the metallization, and the attaching of the applied prior art.

Claim 40 is rejected under 35 U.S.C. 103(a) as being unpatentable over Vinciarelli, Moden and Mazzoni as applied to claim 25, and further in combination with Gaynes (6165885).

Vinciarelli, Moden and Mazzoni do not appear to explicitly disclose applying the heat to reflow the solder using a convection oven.

Nonetheless, at column 21, lines 15-17, Gaynes discloses applying heat to reflow solder using a convection oven. Moreover, it would have been obvious to combine this process of Gaynes with the process of the applied prior art because it would facilitate the reflow of the applied prior art.

Claim 48 is rejected under 35 U.S.C. 103(a) as being unpatentable over Vinciarelli, Moden and Mazzoni as applied to claim 25, and further in combination with Saito (JP63194342).

Vinciarelli, Moden and Mazzoni do not appear to explicitly disclose applying the heat to reflow the solder while maintaining the substrate at a fixed position relative to the chip.

Nevertheless, in the English abstracts and Figures, Saito discloses applying the heat to reflow the solder 4 while maintaining the substrate 1 at a fixed position relative to the chip 3. Furthermore, it would have been obvious to combine this disclosure of Saito with the disclosure of the applied

prior art because it would facilitate the alignment and reflowing of the applied prior art.

Claims 60, 61, 66, 68 and 115-119 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mazzoni (5863406) and Prevotat (5980721).

As cited supra, Mazzoni discloses a method of making a flip chip assembly, comprising the following steps in the sequence set forth: providing a substrate that includes a dielectric layer 110 and a conductive trace 310, 330 wherein the dielectric layer includes first and second surfaces that are opposite one another and a via hole 140 that extends between the first and second surfaces, and the conductive trace includes metallization disposed on walls of the via hole and a bond site disposed on the first surface and spaced from the via hole; depositing solder 340 on the metallization and the bond site, wherein the solder on the metallization is in the via hole, the solder on the bond site is outside the via hole, and the solder on the metallization does not directly contact the solder on the bond site; attaching the substrate to a semiconductor chip "FCA," wherein the first surface faces away from the chip, the second surface faces towards the chip, the chip includes a terminal pad "contacts," the solder on the metallization

contacts the pad, the metallization inherently does not directly contact the pad, and the solder on the bond site does not directly contact the chip; and applying heat to reflow the solder such that the solder on the metallization forms a solder joint that contacts and electrically connects the metallization and the pad, the solder on the bond site forms a solder contact that does not contact the solder joint and does not contact the chip; depositing the solder on the metallization and the bond site using electroplating; wherein the metallization is aligned with the second surface; wherein the metallization and the solder joint are the only materials in the via hole after applying the heat to reflow the solder; wherein the solder joint extends continuously between the first and second surfaces in the via hole; wherein the solder joint is the only material in the via hole that contacts the metallization; wherein the solder joint is the only material in the via hole that contacts the pad; wherein the solder joint is the only material that contacts the metallization and the pad; wherein the solder joint is the only conductor external to the chip that contacts the pad.

However, Mazzoni does not appear to explicitly disclose that the conductive trace electrically connects the solder joint and the solder contact.

Regardless, at column 4, lines 2-25; and column 5, lines 15-48, Prevotat discloses that the conductive trace 2 electrically connects the solder joint 11 and the solder contact ("certain reserved component areas" illustrated in FIG. 10 but not labeled). Moreover, it would have been obvious to combine this disclosure of Prevotat with the disclosure of Mazzoni because Prevotat discloses that it is desirable, and it would enable electrical connection between components on the first and second surfaces.

Claims 69 and 90-94 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mazzoni and Prevotat as applied to claim 60, and further in combination with Moden (5920123).

Mazzoni and Prevotat does not appear to explicitly disclose wherein the pad is directly beneath essentially all surface area defined by the via hole after attaching the substrate to the chip; attaching the substrate to the chip using an adhesive that does not electrically connect the substrate and the chip; attaching the substrate to the chip using an adhesive that is sandwiched between and contacts the substrate and the chip and does not electrically connect the substrate and the chip; wherein the pad is a bumpless pad; wherein the pad is a solder-free pad; wherein the pad is a bumpless solder-free pad.

Notwithstanding, as cited supra, Moden discloses wherein the pad 28 is directly beneath essentially all surface area defined by the via hole after attaching the substrate 12 to the chip 16; attaching the substrate to the chip using an adhesive 27 that does not electrically connect the substrate and the chip; attaching the substrate to the chip using an adhesive 27 that is sandwiched between and contacts the substrate and the chip and does not electrically connect the substrate and the chip; wherein the pad is a bumpless pad; wherein the pad is a solder-free pad; wherein the pad is a bumpless solder-free pad. Moreover, it would have been obvious to combine this disclosure of Moden with the disclosure of the applied prior art because it would facilitate the flip chip assembly of the applied prior art.

Claim 67 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mazzoni and Prevotat as applied to claim 60, and further in combination with Vinciarelli (5516234).

Mazzoni and Prevotat does not appear to explicitly disclose wherein essentially all of the solder joint is in the via hole.

Still, as cited supra, Vinciarelli discloses wherein essentially all of the solder joint 79 is in the via hole 45a. Furthermore, it would have been

obvious to combine this disclosure of Vinciarelli with the disclosure of the applied prior art because it would minimize the assembly size.

Applicant's amendment and remarks filed on 10-1-4 have been fully considered, are addressed by the rejections supra, and are further addressed infra.

Applicant states, "Applicant said nothing about Species 4A and 4B being 'not patentably distinct.'"

This statement is respectfully deemed unpersuasive because it is not maintained in the record that applicant said something about Species 4A and 4B being not patentably distinct. Rather, applicant's statement, "As a result, the claims that read on Species 4A also read on Species 4B and vice-versa," is an implicit admission that the species including substantially all of the solder joint is within the via hole and the solder joint fills a bottom portion of the via hole without filling the top portion are not patentably distinct.

Also, applicant traverses the 35 U.S.C 112, first paragraph rejection of claims 57, 58, 67 and 69 because, "Claims 57, 58, 67 and 69 say nothing about these limitations being 'essential' to the claimed invention."

This traversal is respectfully traversed because the term *essentially* is the adverbial form of the term *essential*, and the relevant definitions of the term *essential* are:

> 1 : of, relating to, or constituting essence
> 2 : of the utmost importance
> synonyms ESSENTIAL, FUNDAMENTAL, VITAL, CARDINAL mean so important as to be indispensable. ESSENTIAL implies belonging to the very nature of a thing and therefore being incapable of removal without destroying the thing itself or its character <conflict is *essential* in drama>. "essential." *Merriam-Webster Online Dictionary*. 2004. http://www.merriam-webster.com (21 Dec. 2004).

Therefore, the limitations introduced by the term *essentially* are essential limitations.

Applicant also traverses the 35 U.S.C. 112, first paragraph, rejection of claims 20, 24, 25, 46, 55, 59, 60, 68, 70, 71, 73-76, 78, 79, 85, 86, 88, 89-91, 93, 94, 96-99, 101-104, 111-114 and 116-119, and cites various portions of the disclosure to support this traversal.

In particular, applicant asserts, "Ablestik Ablebond 961-2 is an electrically insulating epoxy adhesive, as described on the Ablestik Web site (www.ablestik.com)."

This assertion is respectfully traversed because Ablestik Ablebond 961-2 is not described on this website. In any case, there is no original disclosure that the adhesive is not rendered conductive by additional structure such as conductive fillers, or that the adhesive does not otherwise

electrically connect the substrate and the chip. Still further, a disclosure of an insulating adhesive would not provide a basis to exclude a process of attaching the substrate to the chip using an adhesive that electrically connects the substrate and the chip via electromagnetic fields, capacitances and inductances. See Yenzer v. Agrotors Inc. (DC MPa) 20 USPQ2d 1198 (4/23/1991).

The traversal of the 35 U.S.C. 112, first paragraph, rejection of claims 20, 24, 25, 46, 55, 59, 60, 68, 70, 71, 73-76, 78, 79, 85, 86, 88, 89-91, 93, 94, 96-99, 101-104, 111-114 and 116-119, is also respectfully deemed unpersuasive because the cited disclosures do not provide basis for the negative limitations. In particular, it appears that applicant is relying on an absence of a positive recitation in the disclosure as a basis for the negative limitations in the claims. However, as elucidated in the rejection, the mere absence of a positive recitation is not basis for an exclusion. To illustrate, for example, the negative limitation, "without filling a top portion of the via hole after the reflowing," excludes a process of filling a top portion of the via hole after the reflowing, and then removing the top portion; however, there is no basis in the original disclosure for the exclusion of this process. To further illustrate, all of the drawing figures are static "fragmented partial

sectional" views which, as such, do not provide support for exclusion of processes and structure not illustrated.

Relatedly, applicant cites particular disclosures in related patents as support for the negative limitations.

These citations are respectfully deemed unpersuasive because they do not constitute original disclosure. Otherwise, it is respectfully noted that MPEP 1701 admonishes: "Every patent is presumed to be valid, 35 U.S.C. 282, first sentence. Public policy demands that every employee of the Patent and Trademark Office refuse to express to any person any opinion as to the validity or invalidity of, or the patentability or unpatentability of any claim in any U.S. patent." Further, it is well settled that the allowance of claims in one application has no relevancy in the consideration of the question of patentability of claims in another application; In re Greider et al. 54 USPQ 139 [CCPA 1942]. In re Albert C. Fischer 8 USPQ 481 [1931].

Applicant also contends that, "the Office Action fails to acknowledge the Substitute Specification," and further, "requests that the next written communication to Applicant confirm that the Substitute Specification has been entered."

It is respectfully submitted that there is no requirement that an Office action acknowledge entry of a substitute specification. However, in view of applicant's request, and to continue to afford applicant the benefit of compact prosecution, it is confirmed that the substitute specification has been entered.

Applicant further alleges, "the Office Action fails to acknowledge the Submission [Proposed Drawing Amendment, filed on 5-10-1]."

This allegation is respectfully traversed because the form PTOL-326, filed on 9-23-4, acknowledged the submission.

In addition, applicant notes, "The Office Action cover sheet and the footer on pages 2-14 indicate Art Unit 2822. However, the Examiner is with Art Unit 2827."

Applicant is respectfully informed that the indication of Art Unit 2822 and all other identifying information on the cover sheet and footer is correct.

The art made of record and not applied to the rejection is considered pertinent to applicant's disclosure. It is cited primarily to show inventions similar to the instant invention.

have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alternatively, applicant may contact the File Information Unit at (703) 308-2733. Telephone status inquiries should not be directed to the examiner. See MPEP 1730VIC, MPEP 203.08 and MPEP 102.

Any other telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (571) 272-1930. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.
The fax phone number for group 2800 is (703) 872-9306.

David E. Graybill
Primary Examiner
Art Unit 2827

D.G.
22-Dec-04